# A Pilot Study: Introducing HDL Lab Course for Effective Learning of Digital Design

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***Abstract*— Incorporating VHDL programming and implementation using programmable logic devices (PLD) in fundamental digital design course for Electronics Engineering at undergraduate level has become increasingly essential. However it is experienced that integration of VHDL with fundamentals of digital design in one course students give lesser time and importance for VHDL programming. Hence learning objective related to VHDL programming is not achieved up to the expected level. Experience of giving additional training to interested students had shown improvement in students' performance. This paper discusses effect of designing of a separate compulsory laboratory course in VHDL and its effect on the understanding of students and achieving the learning objectives. It also discusses the effect on performance of students in Digital Design course after separating VHDL programming from it. The feedback of students shows that students learn better in laboratory course and they are motivated to learn further in the same area.**

***Keywords— VHDL, engineering education, curriculum design, and digital Logic.***

## I. INTRODUCTION

**DI**GITAL design is a fundamental course of Electronics Engineering. Traditionally the contents of this course include basic combinational and sequential circuits; their design methodologies. The associated laboratory course consists of a few breadboard based experiments on combinational, sequential circuits. Inclusion of hardware description languages (HDL) for learning Digital Design have long been addressed in education literature [1][2][3]. It is found that focus on HDL for learning Digital Design and employing programmable logic enhances the effectiveness of learning process. In [4] the authors have assessed the benefits of using PLD boards in Digital Design course. Considering the essence of use of HDL in digital design course the authors in [5] have focused on teaching Digital System Design in a very innovative project based approach.

Due to advancements in hardware description languages (HDL) and reconfigurable computing (RC), it is essential for every student to have skill of programming in HDL and implementation on reconfigurable logic [6]. The authors have designed curriculum for digital system design with its main focus on FPGA technology and design using VHDL (VHSIC Hardware Description Language).

Work by Yi Zhu et.al, [7] has argued that the use of PLD boards, even for students without much previous hardware experience, can be of significant benefit, as building real hardware allows students to gain a better understanding of the material. Also, students can grasp the full design implementation cycle, which is invaluable in terms of real world experience and students enjoy this kind of learning. However, CPLD board based learning will not give students insight of test benches and simulations.

In the traditional curriculum VHDL was introduced as a programming tool in the curriculum and few introductory experiments on VHDL were conducted in the associated laboratory. But because of integration of VHDL with digital circuit fundamentals, the instructor finds it difficult to devote enough time for teaching and practicing VHDL. Also because of less weightage of VHDL in the course contents and end semester examination many students do not attempt programming. Consequently, the course outcomes related to VHDL programming shows poor attainment. Use of modern tools is also recommended as per ABET criterion in accreditation process.

When a workshop was conducted for interested students to give them additional exposure to learning VHDL in the laboratory, it was found that the students learnt concepts of digital design better than those who were not included in this workshop.

This paper presents steps of curriculum design of a laboratory course for HDL and results of impact on students' performance after undergoing the course for one semester in a self-financed engineering institute affiliated to University of Mumbai, India. The goal is to expose students to power and features of HDL and acquire programming skills useful for digital design. Section II discusses the experiences which instilled the concept of introducing a laboratory course. Section III describes the research questions leading to steps in curriculum design, tools developed and data gathered. Section IV presents the results of continuous assessment during the semester, student feedback and end semester examination followed by conclusion in Section V.

## II. MOTIVATION

Attainment of course outcome of VHDL programming was very poor in University of Mumbai curriculum of Digital Design. As VHDL is one part of the course and introduced

978-1-5090-6115-0/16 $31.00 © 2016 IEEE
DOI 10.1109/T4E.2016.9

towards the end, student find it difficult to learn and practice new topic. Hence they lose interest in use of VHDL in further courses.

To overcome this difficulty following steps were taken by us in past.

### A. Teaching VHDL along with Digital Circuits

In 2014-15 VHDL programming was introduced simultaneously as the students learn different digital circuits, namely combinational circuits like adder, comparator, multiplexer and sequential circuits like counters, shift registers etc. It was with the intention of improving learning outcome.

But even then the numbers of experiments performed were very limited and weightage in end semester examination was very less and hence the outcome was almost same.

### B. Workshop on VHDL

A workshop was conducted for interested students in Semester IV, in consecutive two years (2013-14 and 2014-15)

Approximately 10 sessions, of 2 hours duration were conducted in extra hours. They were given brief overview of VHDL features, writing codes, test benches and simulations. They were also taught implementation on CPLD boards. They performed around 6 experiments while learning.

They were asked to work on a small project to be simulated and implemented within 15 days' time. Study material was given which can also be used by any student.

In both years students participated in this workshop enthusiastically and completed their work successfully. Considering the progress of some of these students in their project work and choice of electives in final year, it is found that they were motivated to use this technology.

But the number was very small (approximately 25 in each year). The reason can be multifold, one may be they are not motivated to work in extra hours and in second year they do not understand the necessity of learning modern technology.

## III. RESEARCH METHOD

The idea of introducing this as a laboratory course was evolved from experiences of these workshops. The students study this course for complete semester (as against 2-3 weeks in University curriculum) and hence they can have enough time to learn step by step and experiment in the laboratory.

In order to study effectiveness of laboratory course following Research Questions are addressed.

RQ1: Do the students perform better in VHDL programming skills and fulfill the course outcomes?

RQ2: Do the students perceive that learning in laboratory course motivates them to take up projects or further courses in the area of digital design?

### A. Sample

290 students of Second year UG engineering in Electronics Engineering (ETRX) and Electronics & Telecommunication Engineering (EXTC) in Autonomous curriculum of a self-financed autonomous institute affiliated to University of Mumbai, India.

Since the students are admitted in two different departments as ETRX and EXTC as per admission guidelines of Department of Technical Education (DTE) two groups are considered for study and analysis. As far as their prerequisite knowledge is concerned they are equivalent groups since they undergo almost same courses in their semester I, II and III.

The sampling is convenience sampling as the researchers are the faculties conducting the HDL laboratory course in their institute.

### B. Procedure

#### 1) Steps in Curriculum Design

For designing the curriculum for HDL laboratory course following steps were taken.

- Define Course outcomes
- Define Course contents
- Choose the PLD boards
- Define rubrics for continuous assessment
- Conduction of Laboratory
- Feedback from students
- End semester Examination

The course was designed during academic year 2014-15, got approved and implemented in 2015-16 for Semester IV Electronics Engineering (ETRX) and Electronics & Telecommunication Engineering (EXTC).

#### 2) Course Outcomes

The students from ETRX and EXTC branches undergo a fundamental course on Digital Design in Semester III. Introduction of this laboratory course is useful to enhance the understanding of logic design. Main goal is to expose students to power and features of VHDL, acquire programming skills and implement in digital design.

Hence the Course outcomes were mainly focusing on ability of students for

1. Writing codes for combinational and sequential circuits using features of VHDL.
2. Debugging, Testing and simulating codes.
3. Implementing the design on PLDs

#### 3) Course Contents

The course was designed with focus on programming practice and use of synthesis and simulation tools in laboratory.

Course contents include

- Basic structure of VHDL code
- Data types supported by VHDL
- Operators, Attributes
- Concurrent and sequential constructs,
- Library and Packages

- Use of functions and procedures
- Writing a Test Bench
- Fundamentals of PLD implementation

The laboratory experiments include

- Programs using concurrent statements like adder, multiplexer, priority encoders etc.
- Programs based on sequential statements like Counters , shift registers
- Programs for FSM implementation
- Programs using functions and procedures

It is expected that the course exposes students to applications of VHDL and its use in implementation of simple mini projects.

*4) Choice of PLD boards*

PLD boards are used for implementation of above experiments and for mini projects. Since most applications were simple, and the codes of small size, Helium CPLD boards with following features were found useful. These educational boards were developed at IIT Bombay in Wadhawani Electronics Laboratory for providing a cost effective solution for Modern Digital Design. These boards can be easily handled by students by referring to the manual provided.

Features of PLD Board:

- Altera MAX3000 CPLD EPM3064 (64 Macro cells, 1250 gates)
- Onboard clock of 1Hz, external clock can be given.
- 8 onboard inputs and 8 onboard outputs

*5) Rubrics for continuous assessment*

Rubrics were designed for continuous evaluation of laboratory work of students. It contained parameters such as VHDL programming skills, testing the design, implementation on CPLD /FPGA and report writing.

*6) Conduction of Laboratory*

For the conduction of this course two groups were considered from Semester IV of the Electronics Engineering (ETRX) and Electronic and telecommunication Engineering (EXTC) of approximately 150 students each in 2015-16 even term.

The ETRX group was given inputs of background theory for one hour once a week and then further subdivided in smaller groups of approximately 18-20 for laboratory performance of 2 hours per week.

The EXTC group was given inputs during laboratory session and then performed experiments in smaller groups of approximately 18-20 for 2 hours per week. The necessary study material was made available in laboratory in the form of E books and PPTs. Instructions were given in lab sessions for use of manual, programming & testing, and implementation on PLD boards.

Examples of Mini Projects by students

- 4 bit ALU
- 4 bit carry look ahead Adder
- Traffic light controller
- Lift controller
- 2 bit multiplier
- Barrel shifter
- Frequency detector
- Sequential pulse generator
- Vending machine controller
- Watchdog Timer
- Code convertors
- Electronic piano

*7) Student Feedback*

At the end of semester, survey questionnaire was administered through Google form. The students were given two week duration for completion of the survey. They completed the survey individually without any bias of peer or faculty.

*8) End Semester Examination*

At the end of the semester all the students have to appear for the practical examination which focused on their VHDL programming skills.

*9) Continuation Audit Course*

There is a continuation audit course offered in their Semester V, namely reconfigurable logic design, in which they will work more on CPLD / FPGA based projects.

*C. Instruments*

The instruments used for the study are

1) Survey questionnaire
2) Rubrics for continuous evaluation
3) End semester practical examination
4) Choice form for audit course

*1) Survey Questionnaire*

After defining the research questions, scope, target audience and methodology, the survey instrument was developed in the form of a paper-based questionnaire for maximum flexibility. This was then converted to online Google form. The design process was conducted by the engineering faculties. The questionnaire was reviewed, validated and revised before external release.

TABLE I. SURVEY STRUCTURE AND LENGTH

| Sr. No | Section Title | No of Questions | Type of Questions | |
|---|---|---|---|---|
| | | | ***Four Point Likert Scale*** | ***Open Ended*** |
| 1 | Ability to use VHDL features | 5 | 5 | |
| 2 | Ability to write test benches and simulate | 2 | 2 | |
| 3 | CPLD Implementations | 2 | 2 | |
| 4 | Comparison with traditional classroom teaching | 1 | 1 | |
| 5 | Motivation and Preparedness | 2 | | 2 |

*2) Rubrics for continuous evaluation*

This instrument was designed by the faculty, validated and reviewed before giving to the students. The focus of this instrument was course outcomes defined. It contained parameters such as

- Programming Skills (Writing Code using VHDL features for given task.)
- Testing the design (Writing Test Bench and interpretation of simulation results.)
- Implementation on CPLD /FPGA(Assignment of pins and implementation on CPLD/ FPGA, testing on the hardware)
- Report writing and submission

It was used for evaluation of the skills of students during laboratory work. A faculty gives marks for each laboratory session in the range of 0 to 25 on the basis of rubrics designed. A course outcome is attained when a student scores more than 60% marks.

*3) End semester practical examination*

This was practical examination where each student was asked to write VHDL program for a digital design problem and show simulation results or implement the same on CPLD board. There was a viva based on the curriculum. A course outcome is attained when a student scores more than 60% marks.

*4) Choice form for audit course*

Google form for choice of audit course was designed at institute level , where students had to fill the choices in order or prefernce.

### D. Data Gathered

The following data was gathered for analysis at the completion of the study.

1) The marks obtained by students of ETRX and EXTC in semester evaluation of laboratory work.

2) The marks obtained by the students of ETRX and EXTC in the end semester practical examination.

3) Student responses to the four point Likert scale questions

4) Students responses to open ended question

5) The marks obtained by students of ETRX and EXTC in end semester theory examination of Digital Design (Semester III) in 2014-15(Control group) and 2015-16 (Experiment group)

6) Student response to audit course choice form.

### E. Data Analysis Techniques

*1) Continuous evaluation of laboratory work.*

The marks obtained during laboratory work are analyzed for course outcome attainment. A course outcome is attained when a student scores more than 60% marks.

*2) End semester practical examination.*

From the marks obtained by students in end semester practical examination percentage of students scoring above 80% (High performers) and scoring in range of 60 to 80 % (medium performers) are found. Students in the range of 40 to 60 % are not considered, though they have passed the examination, as they have not acquired the skills up to the expectations.

*3) Student Feedback*

- Four point likert scale questions
- Open ended question

*4) Comparison with previous results*

The marks obtained by students of ETRX and EXTC in end semester theory examination of Digital Design (Semester III) in 2014-15(control group) and 2015-16 (experiment group)

An independent T test was conducted for ETRX and EXTC group to evaluate the hypothesis and validate the results.

## IV. RESULTS

### A. Continuous evaluation of laboratory work.

The marks obtained during laboratory work including mini projects are analyzed for course outcome attainment.

TABLE II. CONTINUOUS EVALUATION

| **Parameter for Evaluation** | **% of Students above 60% During Semester Laboratory work** | |
|---|---|---|
| | ***EXTC*** | ***ETRX*** |
| Writing codes for combinational and sequential circuits using features of VHDL. | 82 | 60 |
| Debugging, Testing and simulating codes. | 82 | 59 |
| Implementing the design on PLDs | 84 | 33 |

By doing mini projects students experienced applications in digital design.

### B. End semester practical examination.

Students are categorized as High performers (above 80%) and medium performers (60 to 80 %) in end semester practical examination. From the graph it is seen that percentage of students in these categories is substantially high, as 82 % in EXTC and 62 % in ETRX.

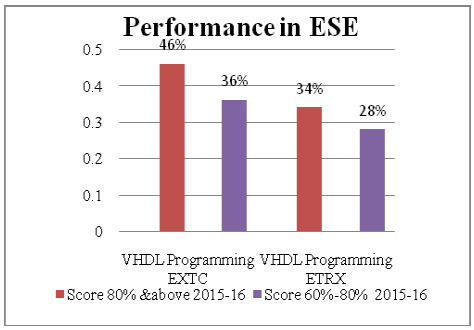


Fig. 1. Performance of Students in End Semester Examination

The same VHDL code writing skills when compared with ESE of year 2014 when VHDL was integrated with DLD course it is seen that all students do not attempt the question and only few students' score good marks

TABLE III. PERFORMANCE IN 2014-15

| Parameter of evaluation in 2014-15 | % of students | | |
|---|---|---|---|
| | *Attempting* | *Scoring above 80%* | *Scoring in 60 - 80%* |
| VHDL Programming EXTC | 37 | 8 | 21 |
| VHDL Programming ETRX | 31 | 6 | 10 |

### C. Student Feedback

*1) Four point Likert scale questions :*

TABLE IV. STUDENTS PERCEPTION ON COURSE OUTCOMES

| Course Outcome | % of students Strongly Agree | | % of students Agree | | % of students Disagree | |
|---|---|---|---|---|---|---|
| | EXTC | ETRX | EXTC | ETRX | EXTC | ETRX |
| Able to write code using VHDL constructs for combinational and sequential circuits | 38 | 32 | 60 | 65 | 2 | 3 |
| Able to simulate the system described in VHDL using test benches or built in simulators | 30 | 56 | 63 | 42 | 7 | 2 |
| Realize the system described in VHDL on CPLD/FPGA | 46 | 6 | 51 | 66 | 3 | 28 |

*2) Open ended question:*

From the feedback of students it is very clear that more than 90% of students feel that learning by experimentation is better than traditional classroom learning; about 40% students very strongly feel so. About 80% students are willing to take up further courses or projects in this area. And about 75% students feel that they are equipped for this activity from this course.

### D. Comparison with previous results

When the results of DLD in 2014-15 (when VHDL is integrated with DLD course in Mumbai university curriculum) and results of DLD in 2015-16 (when HDL separate course autonomous curriculum) it is seen that the average marks of students increase whereas there is marginal increase in number of students scoring higher marks.

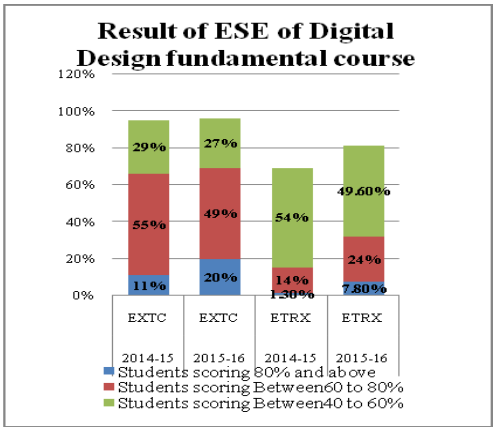


Fig. 2. Comparison of DLD results in ESE of 2014-15 and 2015-16

TABLE V. RESULT OF T TEST

| | EXTC | | ETRX | |
|---|---|---|---|---|
| | *2014-15* | *2015-16* | *2014-15* | *2015-16* |
| No of Students | 153 | 146 | 149 | 140 |
| Mean | 63.1 | 65.7 | 44.2 | 53.7 |
| Standard deviation | 15.7 | 14.1 | 15.3 | 16.9 |
| Value of T | -1.52 | | -5.03 | |
| P | 0.064 | | <0.0001 | |

In order to ascertain the statistical significance of result of ESE, we formulated a hypothesis and performed paired sample t-test to prove or disprove our hypothesis.

The null hypothesis can be stated as:

H0: $\mu 1 = \mu 2$: the laboratory course didn't cause any change in students' performance.

The alternate hypothesis is:

H1: $\mu 1 \neq \mu 2$: The laboratory course did cause a change in students' performance.

The result of t-test is tabulated in Table 5. From Table 5, we observe that the test is statistically significant and hence, we can reject the null hypothesis.

### E. Choice for audit course

The audit course namely reconfigurable logic design is opted by approximately 40 students for 2016-17. This indicates that they not only feel, but are actually ready to work in the field.

## V. DISCUSSION AND CONCLUSION

Through this study we try to find answer to the following research questions

RQ1: Do the students perform better in VHDL programming skills and fulfill the course outcomes?

From the evaluation of work during the semester it is found that more than 60% students are very good in writing codes, testing and implementing on CPLD.

From end semester evaluation also it is clearly visible that students have improved in their performance as compared to previous year. The analysis of results indicates that average marks have increased whereas there is marginal increase in number of students scoring higher marks.

Hence the course outcomes are attained satisfactorily which was not possible in University curriculum.

RQ2: Do the students perceive that learning in laboratory course motivates them to take up projects or further courses in the area of digital design?

In the response of survey conducted, more than 90% of students feel that learning by experimentation is better than traditional classroom learning. About 80% students are willing to take up further courses or projects in this area.

From the registration of the audit course on reconfigurable logic design it is obvious that more students are motivated to work in this area.

The course was implemented from January 2016 and hence the observations are based on our first experience. It will not be appropriate to concretely put forth these observations as conclusions. They can be substantiated only after sufficient time.

In the survey conducted, students have expressed that they need more experimentation, or hands on sessions. Some have said that they need more theoretical inputs for understanding features of VHDL. In the class of EXTC especially where theory lecture was not conducted separately, it can be added. In class of ETRX more stress can be given on implementation on CPLD.

## ACKNOWLEDGEMENT

We would like to thank Wadhawani Electronics Laboratory at IIT Bombay for providing us Helium CPLD boards free of cost. This course was jointly conducted by additional six faculty members in ETRX and EXTC departments of K.J. Somaiya College of Engineering, Mumbai. We are grateful to our principal Dr. Shubha Pandit, for continuous encouragement and suggestions. We are thankful to Mrs. Anita Diwakar from department of Education Technology, IIT Bombay, for mentoring us during the process of paper writing.

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